IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A compander comprising

an input signal,

an input detector for detecting a predetermined condition of the input signal,

gain calculate logic responsive to the input signal and the input detector for generating a gain signal including a gain value, and

a synchronizer ~~logic~~ responsive to the input detector and the gain signal for synchronizing the input signal and the gain signal to provide an output signal, wherein the predetermined condition of the input signal includes at least one of a zero crossing and a failure to have a zero crossing within a predetermined period.

2. (Currently amended) The compander of claim 1 wherein the synchronizer ~~logic~~ includes a gain cell.

3. (Currently amended) The compander of claim 2 wherein the synchronizer ~~logic~~ further includes a synchronizer block.

4. (Previously presented) The compander of claim 3 wherein the synchronizer block provides a synchronized gain signal and a delayed input signal to the gain cell, and the gain cell output is the output signal.

5. (Previously presented) The compander of claim 1 wherein the gain signal is generated only after the predetermined condition of the input signal occurs.

6. (Currently amended) The compander of claim 5 wherein ~~the predetermined condition of~~ the input signal ~~includes~~ and the gain signal are synchronized to a zero crossing of the input signal.

7. (Currently amended) The compander of claim 6 wherein ~~the predetermined condition of~~ the input signal ~~further includes a~~ and the gain signal are synchronized upon detection of the failure to have a zero crossing within [[a]] the predetermined period.

8. (Previously presented) The compander of claim 5 further including
monitor logic for monitoring the input signal,
power estimator logic responsive to the monitor logic for providing the gain signal.

9. (Original) The compander of claim 8 wherein the monitor logic initiates monitoring on the occurrence of the predetermined condition.

10. (Original) The compander of claim 8 wherein the monitor logic terminates monitoring on the occurrence of the predetermined condition.

11. (Previously presented) The compander of claim 9 wherein the monitor logic generates at least one signal value and periodically passes the at least one signal value to the power estimator logic.

12. (Previously presented) The compander of claim 10 wherein the monitor logic generates at least one signal value and passes the at least one generated signal value to the power estimator logic upon occurrence of the predetermined condition.

13. (Original) The compander of claim 11 wherein the generated signal value is the peak signal.

14. (Original) The compander of claim 11 wherein the generated signal is the average signal.

15. (Original) The compander of claim 11 wherein the generated signal is the RMS signal.

16. (Original) The compander of claim 12 wherein the generated signal is the peak signal.

17. (Original) The compander of claim 12 wherein the generated signal is the average signal.

18. (Original) The compander of claim 12 wherein the generated signal is the RMS signal.

19. (Original) The compander of claim 12 wherein the monitor logic resets upon occurrence of the predetermined condition.

20. (Previously presented) The compander of claim 8 wherein the power estimator logic includes initial power estimator logic for determining an initial power estimate, and
variable attack and release logic responsive to the initial power estimate for determining a rate of change for the gain signal.

21. (Original) The compander of claim 20 wherein the initial power estimate includes a plurality of initial power estimates.

22. (Original) The compander of claim 21 wherein the variable attack and release logic comprises a plurality of variable attack and release modules.

23. (Original) The compander of claim 20 wherein the initial power estimator logic provides at least first and second power estimator signals, and wherein the variable attack and release logic compares the first power estimator signal with the second power estimator signal.

24. (Original) The compander of claim 20 wherein the initial power estimator logic provides at least one power estimator signal to the variable attack and release logic and the output of the variable attack and release logic is fed back to provide a second input to the variable attack and release logic.

25. (Previously presented) The compander of claim 23 wherein the second power estimator signal is provided by the initial power estimator logic which receives as an input the output of the variable attack and release logic.

26. (Canceled)

27. (Withdrawn) A signal processor comprising

a first input representative of a time between events,

a computation engine responsive to the first input and capable of supplying an equalization value in accordance with the first input,

a second input representative of a signal characteristic associated with the time between events, and

combiner logic for combining the equalization value with the second input.

28. (Withdrawn) The signal processor of claim 27 wherein the computation engine is a lookup table.

29. (Withdrawn) The signal processor of claim 27 wherein the computation engine is a processor.

30. (Withdrawn) The signal processor of claim 29 wherein the processor includes an algorithm to perform an appropriate computation for the computation engine.

31. (Withdrawn) The signal processor of claim 29 wherein the processor includes digital logic.

32. (Withdrawn) The signal processor of claim 30 wherein the algorithm includes a plurality of computer program steps.

33. (Withdrawn) The signal processor of claim 27 wherein a plurality of the second inputs is received during the time between events.

34. (Withdrawn) A signal processor comprising

a first input representative of a time between events,

a computation engine responsive to the first input and capable of supplying filter parameters in accordance with the first input,

a second input representative of a signal characteristic associated with the time between events, and

a filter responsive to the filter parameters for processing the second input.

35. (Withdrawn) The signal processor of claim 34 wherein the filter includes a plurality of filters.

36. (Withdrawn) The signal processor of claim 35 wherein the second input includes a plurality of inputs and each of the plurality of filters responds to an associated one of the plurality of inputs.

37. (Withdrawn) The signal processor of claim 34 wherein the second input is equalized.

38. (Withdrawn) The signal processor of claim 34 wherein the computation engine is a lookup table.

39. (Withdrawn) The signal processor of claim 34 wherein the computation engine is a processor.

40. (Withdrawn) The signal processor of claim 34 wherein the processor includes an algorithm to perform an appropriate computation for the computation engine.

41. (Withdrawn) The signal processor of claim 39 wherein the processor includes digital logic.

42. (Withdrawn) The signal processor of claim 40 wherein the algorithm includes a plurality of computer program steps.

43. (Withdrawn) The signal processor of claim 34 wherein a plurality of the second inputs is received during the time between events.

44. (Currently amended) A compander having

an input comprising a plurality of power estimator signals, and

a first signal processing stage for processing the plurality of power estimator signals

wherein the compander provides an output by synchronizing a first signal and a gain signal based on detection of a predetermined condition of the first signal, the predetermined condition including at least one of a zero crossing and a failure to have a zero crossing within a predetermined period.

45. (Original) The compander of claim 44 wherein the processing is demodulating.

46. (Original) The compander of claim 44 wherein the processing is filtering.

47. (Canceled)

48. (Previously presented) The compander of claim 44 wherein the processing is combining of at least some of the plurality of power estimator signals.

49. (Previously presented) The compander of claim 44 wherein the processing is selecting a preferred one of the plurality of power estimator signals.

50. (Currently amended) A device comprising a compander having

a first input comprising at least one local power estimator signal,

a second input comprising at least one external power estimator signal,

a first signal processor for processing the first input and the second input to produce a power estimate, wherein

the compander provides an output by synchronizing a first signal and a gain signal based detection of a predetermined condition of the first signal, the predetermined condition including at least one of a zero crossing and a failure to have a zero crossing within a predetermined period.

51. (Previously presented) The device of claim 50 wherein the processing includes combining the first and second inputs.

52. (Previously presented) The device of claim 50 wherein the processing includes selecting one of the first and second inputs.

53. (Previously presented) The device of claim 50 wherein the processing includes scaling at least one of the first and second inputs.

54. (Previously presented) The device of claim 50 wherein the second input comprises a plurality of external power estimator signals, and further including a second signal processor for processing the plurality of external power estimator signals to produce a single output signal to the first signal processor.

55. (Previously presented) The device of claim 54 wherein the processing performed by the second signal processor includes combining at least some of the plurality of external power estimator signals.

56. (Previously presented) The device of claim 54 wherein the processing performed by the second signal processor includes selecting among at least some of the plurality of external power estimator signals.

57. (Previously presented) The device of claim 54 wherein the processing performed by the second signal processor includes scaling at least one of the plurality of external power estimator signals.

58. (Previously presented) The device of claim 54 wherein the processing performed by the second signal processor includes demodulating at least one of the plurality of external power estimator signals.

59. (Previously presented) The device of claim 54 wherein the processing performed by the second signal processor includes filtering at least one of the plurality of external power estimator signals.

60. (Previously presented) The device of claim 50 wherein the first input comprises a plurality of local power estimator signals, and further including a third signal processor for

processing the plurality of local power estimator signals to produce an exported power estimator signal.

61. (Previously presented) The device of claim 60 wherein the third signal processor comprises a plurality of signal processors, each of which produces an exported power estimator signal.

62. (Previously presented) The device of claim 60 wherein the processing performed by the third signal processor includes combining at least some of the plurality of local power estimator signals.

63. (Previously presented) The device of claim 60 wherein the processing performed by the third signal processor includes selecting among at least some of the plurality of local power estimator signals.

64. (Previously presented) The device of claim 60 wherein the processing performed by the third signal processor includes scaling at least one of the plurality of local power estimator signals.

65. (Previously presented) The device of claim 60 wherein the processing performed by the third signal processor includes modulating at least one of the plurality of local power estimator signals.

66. (Previously presented) The device of claim 60 wherein the processing performed by the third signal processor includes filtering at least one of the plurality of local power estimator signals.

67. (Previously presented) The device of claim 50 further including a second signal processor for processing the second input signal and a third signal processor for processing the first input signal to produce an exported power estimator signal.

68. (Previously presented) The device of claim 67 wherein the second input comprises a plurality of external power estimator signals and the second signal processor processes at least one of the external power estimator signals to produce a single output signal to the first signal processor.

69. (Previously presented) The device of claim 68 wherein the first input comprises a plurality of local power estimator signal, and the third signal processor processes the plurality of local power estimator signals to produce an exported power estimator signal.

70. (Previously presented) The device pander of 67 wherein the processing performed by the second signal processor includes demodulating the second input signal, and the processing performed by the third signal processor including modulating the first input signal.

71. (Previously presented) The device of claim 68 wherein the processing performed by the second and third signal processors is selected from a group including modulating, demodulating, scaling, selecting, combining and filtering.

72. (Currently amended) A signal processing method for use with companders comprising the steps of

providing at least one local power estimator signal,

providing at least one external power estimator signal,

signal processing the local power estimator signal and the external power estimator signal to produce a power estimate, wherein

the compander provides an output by synchronizing a first signal and a gain signal based detection of a predetermined condition of the first signal, the predetermined condition including at least one of a zero crossing and a failure to have a zero crossing within a predetermined period.

73. (Original) The signal processing method of claim 72 wherein the external power estimator signal comprises a plurality of secondary external power estimator signals, and further including the step of signal processing the plurality of secondary external power estimator signals to produce the external power estimator signal.

74. (Previously presented) The compander of claim 8 further including

a first plurality of power estimator signals, and

a processing stage for combining at least some of the first plurality of power estimator signals and for generating at least one output signal.

75. (Currently amended) A compander having

a first external power estimator signal,

a second external power estimator signal,

a first signal processor for processing the first and second power estimator signals to produce a first output wherein processing includes at least one of a group comprising scaling, combining and selecting the first and second power estimator signals, wherein the compander provides an output by synchronizing a first signal and a gain signal based detection of a predetermined condition of the first signal, the predetermined condition including at least one of a zero crossing and a failure to have a zero crossing within a predetermined period.

76. (Original) The compander of claim 75 wherein the processing includes demodulating at least one of the external power estimator signals.

77. (Original) The compander of claim 75 wherein the processing includes scaling at least one of the external power estimator signals.

78. (Original) The compander of claim 75 wherein the processing includes filtering at least one of the external power estimator signals.

79. (Original) The compander of claim 75 further including a second signal processor for processing the first output.

80. (Original) The compander of claim 79 wherein the second signal processor modulates the first output.

81. (Original) The compander of claim 79 wherein the second signal processor scales the first output.

82. (Original) The compander of claim 79 wherein the second signal processor filters the first output.

83. (Currently amended) A compander comprising

an input signal,

gain calculate logic responsive to the input signal for calculating a gain calculate signal,

a synchronizer ~~logic~~ responsive to the input signal and the gain calculate signal for synchronizing the input signal and the gain calculate signal to provide an output ~~signal.~~ signal,

monitor logic for monitoring the input signal,

power estimator logic responsive to the monitor logic for providing the gain calculate signal,

a first input representative of a time between events,

a computation engine responsive to the first input and configured to supply an initial power estimate in accordance with the first input,

a second input representative of a signal characteristic associated with the time between events, and

combiner logic for combining the initial power estimate with the second input for producing an initial power estimate, and ~~wherein~~

~~the gain calculate logic includes~~ detection logic for detecting a predetermined condition of the input signal, ~~and~~ wherein

the gain calculate signal is generated only after the predetermined condition of the input signal occurs, wherein the predetermined condition includes at least one of a zero crossing and a failure to have a zero crossing within a predetermined period.

84. (Previously presented) The compander of claim 83 wherein the computation engine is a lookup table.

85. (Previously presented) The compander of claim 83 wherein the computation engine is a processor.

86. (Previously presented) The compander of claim 85 wherein the processor includes an algorithm to perform an appropriate computation for the computation engine.

87. (Previously presented) The compander of claim 85 wherein the processor includes digital logic.

88. (Previously presented) The compander of claim 86 wherein the algorithm includes a plurality of computer program steps.

89. (Previously presented) The compander of claim 83 wherein a plurality of the second inputs is received during the time between events.

90. (Currently amended) A compander comprising

an input signal,

gain calculate logic responsive to the input signal for calculating a gain calculate signal,

a synchronizer ~~logic~~ responsive to the input signal and the gain calculate signal for synchronizing the input signal and the gain calculate signal to provide an output ~~signal.~~ signal,

monitor logic for monitoring the input signal,

power estimator logic responsive to the monitor logic for providing the gain signal,

a first input representative of a time between events,

a computation engine responsive to the first input and configured to supply filter parameters in accordance with the first input,

a second input representative of a signal characteristic associated with the time between events, and

a filter responsive to the filter parameters for processing the second input for producing an initial power estimate, and ~~wherein~~

~~the gain calculate logic includes~~ detection logic for detecting a predetermined condition of the input signal, ~~and~~ wherein

the gain calculate signal is generated only after the predetermined condition of the input signal occurs, and wherein the gain signal includes a gain value, wherein the predetermined condition includes at least one of a zero crossing and a failure to have a zero crossing within a predetermined period.

91. (Previously presented) The compander of claim 90 wherein the filter includes a plurality of filters.

92. (Previously presented) The compander of claim 91 wherein the second input includes a plurality of inputs and each of the plurality of filters responds to an associated one of the plurality of inputs.

93. (Previously presented) The compander of claim 90 wherein the second input is equalized.

94. (Previously presented) The compander of claim 90 wherein the computation engine is a lookup table.

95. (Previously presented) The compander of claim 90 wherein the computation engine is a processor.

96. (Previously presented) The compander of claim 90 wherein the processor includes an algorithm to perform an appropriate computation for the computation engine.

97. (Previously presented) The compandcr of claim 95 wherein the processor includes digital logic.

98. (Previously presented) The compander of claim 96 wherein thc algorithm includes a plurality of computer program steps.

99. (Previously presented) The compandcr of claim 90 wherein a plurality of the second inputs is received during the time between events.

100. (Previously prescnted) The compander of claim 11, wherein the generated signal valuc is representativc of a time between occurrence of predetermined conditions.

101. (Previously presented) The compander of claim 12, wherein the generated signal valuc is representative of a time between occurrence of predetermined conditions.

102. (Currently amended) A compandèr comprising

an input signal,

an input detector for detecting a predetermined condition of the input signal,

gain calculate logic responsive to the input signal and the input detector for calculating a gain signal, the gain signal including a gain value,

a synchronizer ~~logic~~ responsive to the input detector and the gain signal for synchronizing the input signal and the gain signal to provide an output signal,

monitor logic for monitoring the input signal,

power estimator logic responsive to the monitor logic for providing the gain signal,

a first input representative of a time between events,

a computation engine responsive to the first input and configured to supply an initial power estimate in accordance with the first input,

a second input represcntative of a signal characteristic associated with the time between events, and

combiner logic for combining the initial power estimatc with the second input for producing an initial power estimate, wherein

the gain signal is generated only after the predetermined condition of the input signal occurs.

103. (Previously presented) The compander of claim 102 wherein the computation engine is a lookup table.

104. (Previously presented) The compander of claim 102 wherein the computation engine is a processor.

105. (Previously presented) The compander of claim 104 wherein the processor includes an algorithm to perform an appropriate computation for the computation engine.

106. (Previously presented) The compander of claim 104 wherein the processor includes digital logic.

107. (Previously presented) The compander of claim 105 wherein the algorithm includes a plurality of computer program steps.

108. (Previously presented) The compander of claim 102 wherein a plurality of the second inputs is received during the time between events.

109. (Currently amended) A compander comprising

an input signal,

an input detector for detecting a predetermined condition of the input signal,

gain calculate logic responsive to the input signal and the input detector for calculating a gain signal,

a synchronizer ~~logic~~ responsive to the input signal and the gain signal for synchronizing the input signal and the gain signal to provide an output ~~signal.~~ signal,

monitor logic for monitoring the input signal,

power estimator logic responsive to the monitor logic for providing the gain signal,

a first input representative of a time between events,

a computation engine responsive to the first input and configured to supply filter parameters in accordance with the first input,

a second input representative of a signal characteristic associated with the time between events, and

a filter responsive to the filter parameters for processing the second input for producing an initial power estimate, wherein

the gain signal is generated only after the predetermined condition of the input signal occurs, and wherein the gain signal includes a gain value.

110. (Previously presented) The compander of claim 109 wherein the filter includes a plurality of filters.

111. (Previously presented) The compander of claim 110 wherein the second input includes a plurality of inputs and each of the plurality of filters responds to an associated one of the plurality of inputs.

112. (Previously presented) The compander of claim 109 wherein the second input is equalized.

113. (Previously presented) The compander of claim 109 wherein the computation engine is a lookup table.

114. (Previously presented) The compander of claim 109 wherein the computation engine is a processor.

115. (Previously presented) The compander of claim 114 wherein the processor includes digital logic.

116. (Previously presented) The compander of claim 114 wherein the processor includes an algorithm to perform an appropriate computation for the computation engine.

117. (Previously presented) The compander of claim 116 wherein the algorithm includes a plurality of computer program steps.

118. (Previously presented) The compander of claim 109 wherein a plurality of the second inputs is received during the time between events.